WHAT IS CLAIMED IS:

1. A method of processing semiconductor substrates and reducing particle contamination and/or process drift during consecutive processing of the substrates, the method comprising steps of:

(a) placing a substrate on a substrate holder in an interior space of a plasma processing chamber, the processing chamber including at lease one slip cast part having a surface exposed to the interior space, the slip cast part having free silicon contained therein and a protective layer on the surface which protects the silicon from being attacked by the plasma in the interior space;

(b) processing the substrate by supplying process gas to the processing chamber and energizing the process gas into a plasma state in the processing chamber, the slip cast part being exposed to the plasma and optionally providing a ground path for RF current sustaining the plasma;

(c) removing the substrate from the processing chamber; and

(d) consecutively processing additional substrates in the processing chamber by repeating steps (a-c) while minimizing particle contamination of the substrates and/or reducing process drift during the processing step as a result of protecting the free silicon from attack by the plasma.

2. The method according to Claim 1, wherein the slip cast part comprises a liner within a sidewall of the processing chamber, the processing chamber including a substantially planar antenna which energizes the process gas into the plasma state by supplying RF power to the antenna and the process gas comprising one or more hydrofluorocarbon gases.

3. The method according to Claim 1, wherein the plasma comprises a high density plasma and the substrates are processed by etching an oxide layer on

the substrates with the high density plasma while supplying an RF bias to the substrates.

4. The method according to Claim 1, wherein the slip cast part comprises a liner within a sidewall of the processing chamber, a gas distribution plate supplying the process gas to the processing chamber, a perforated baffle extending between the substrate holder and an inner wall of the processing chamber, a wafer passage insert and/or a focus ring surrounding the substrate.

5. The method according to Claim 1, wherein the slip cast part comprises a wafer passage insert fitted in an opening in a ceramic liner within a sidewall of the processing chamber, the liner being heated by a heater which maintains the liner at a desired temperature.

6. The method according to Claim 1, wherein the slip cast part consists essentially of silicon impregnated slip cast SiC coated with CVD SiC.

7. The method according to Claim 1, wherein the slip cast part comprises a heated liner and a baffle, the liner surrounding the substrate holder and the baffle comprising a foraminous ring extending between the liner and the substrate holder, the liner being heated to a temperature above room temperature during the processing step.

8. The method according to Claim 1, wherein the slip cast part comprises a gas distribution plate having a resistivity high enough to allow RF energy to pass therethrough, the process gas being energized by an antenna which couples RF energy into the chamber through the gas distribution plate.

9. The method according to Claim 8, wherein the slip cast part further comprises a chamber liner having a resistivity below 200 Ω·cm.

10. A plasma processing system useful for processing semiconductor substrates comprising:

a plasma processing chamber having an interior space bounded by a chamber sidewall;

a substrate support on which a substrate is processed within the interior space, the chamber sidewall being spaced outwardly of a periphery of the substrate support;

a gas supply through which process gas can be supplied to the interior space during processing of the substrate;

an energy source which can energize the process gas in the interior space into a plasma state during processing of the substrate;

a slip cast part having a surface thereof exposed to the interior space, the slip cast part having free silicon contained therein and a protective layer on the surface which protects the silicon from being attacked by the plasma in the interior space.

11. The plasma processing system of Claim 10, wherein the slip cast part is of porous silicon carbide backfilled with silicon.

12. The plasma processing system of Claim 10, wherein the protective layer is a chemical vapor deposited layer of silicon carbide.

13. The plasma processing system of Claim 10, wherein the slip cast part is a wafer passage insert of a plasma etch reactor.

14. The plasma processing system of Claim 10, wherein the gas supply supplies a fluorocarbon and/or a fluorohydrocarbon to the interior space.

15. The plasma processing system of Claim 10, wherein the slip cast part is bonded to the chamber by an elastomer joint.

16. The plasma processing system of Claim 10, wherein the chamber includes a ceramic liner between the chamber sidewall and the substrate support and the slip cast part comprises a tubular liner in an opening extending through the liner.

17. The plasma processing system of Claim 10, wherein the energy source comprises an antenna which inductively couples radiofrequency energy through a dielectric member into the chamber.

18. The plasma processing system of Claim 10, wherein the interior of the chamber is bounded by a showerhead having a silicon carbide extending across the top of the chamber, a liner having a silicon carbide surface extending downwardly from the silicon carbide surface of the showerhead, a plasma screen having a silicon carbide surface extending inwardly from the silicon carbide surface of the liner, and the slip cast part comprising a wafer passage insert fitted in an opening in the liner, the CVD SiC coating forming a surface of the wafer passage insert through which a semiconductor wafer passes into and out of the chamber.